

REMARKS

New claims 12-18 have been added. Support for the new claims may be found in Figures 1 and 3 and related discussion in the specification. No new matter has been added. Thus, claims 1-18 are pending in the present application.

In the Office Action, claims 1-3 were rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Durec (U.S. Patent No. 6,144,846), hereinafter referred to as Durec '846. Applicants note that the filing date of the present application is July 13, 2001 and the issue date of Durec '846 is November 7, 2000. The Examiner's rejections are respectfully traversed.

Durec '846 describes a frequency translation circuit 10 that translates an incoming reference signal to a lower frequency using a compound mixer circuit 42 that includes at least two mixers 14A-X. See Durec '846, Figures 1 and 4 and related discussion. The mixers 14A-X described in Durec '846 each comprise four interconnected transistors 66, 68, 70, 72. However, Durec '846 fails to teach or suggest a multiplier circuit having a first and a second mixer, the first mixer comprising a first number of transistors and the second mixer comprising a second number of transistors, the first number being different than the second number, as set forth in claim 1. For example, Durec '846 fails to teach or suggest that the multiplier circuit comprises a Gilbert cell where all transistors are used as switches, as set forth in claim 13. For at least this reason, Applicants respectfully submit that claims 1-3 are not anticipated by Durec '846 and request that the Examiner's rejections of these claims be withdrawn.

In the Office Action, claims 4-6, 8, and 10-11 were rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Durec (U.S. Patent No. 6,144,845), hereinafter referred to as Durec '845. Applicants note that the filing date of the present application is July 13, 2001 and the issue date of Durec '845 is November 7, 2000. Claims 7 and 9 were rejected under 35 U.S.C.

§ 103(a) as allegedly being unpatentable over Durec '845 in view of Durec '846. The Examiner's rejections are respectfully traversed.

Durec '845 describes an image rejection circuit 10 that receives an incoming signal and an oscillator signal generated by a local oscillator and generates output signals using mixers 14, 24, 34, 44. See Durec '845, Figure 1 and related discussion. The mixers 14, 24, 34, 44 described in Durec '845 each comprise four interconnected transistors 66, 68, 70, 72. However, Durec '845 fails to teach or suggest a first multiplier circuit having a first and a second mixer, the first mixer comprising a first number of transistors and the second mixer comprising a second number of transistors, the first number being different than the second number, as set forth in claim 4. Durec '845 also fails to teach or suggest a second multiplier circuit having a third and a fourth mixer, the third mixer comprising a third number of transistors and the fourth mixer comprising a fourth number of transistors, the third number being different than the fourth number, as set forth in claim 4. For example, Durec '845 fails to teach or suggest that the first and second multiplier circuits comprise Gilbert cells where all transistors are used as switches, as set forth in claim 5. For at least this reason, Applicants respectfully submit that claims 4-6, 8, and 10-11 are not anticipated by Durec '845 and request that the Examiner's rejections of these claims be withdrawn.

Moreover, Applicants respectfully submit that the present invention is not obvious over Durec '845 and Durec '846, either alone or in combination. To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. As discussed above, the cited references fail to teach or suggest multiplier circuits having a first mixer comprising a first number of transistors and a second mixer comprising a second number of transistors, the first number being different than the second

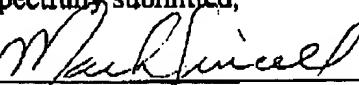
number, as set forth in claims 1 and 4. Moreover, the cited references do not provide any suggestion or motivation to modify the prior art to arrive at Applicants claimed invention. In contrast, the cited references appear to teach away from a multiplier circuit having two mixers with an unequal number of transistors. For example, the four transistors in each of the mixers described in Durec '845 and Durec '846 are interconnected in a manner that appears to require the presence of all four transistors in each mixer. Furthermore, the mixers described in Durec '845 and Durec '846 appear to be interconnected with each other in a manner that requires that each mixer have the same number of transistors as the other mixers. It is by now well established that teaching away by the prior art constitutes *prima facie* evidence that the claimed invention is not obvious. For at least the aforementioned reasons, Applicants respectfully submit that the present invention is not obvious over the cited references, either alone or in combination, and request that the Examiner's rejections of claims 7 and 9 under 35 U.S.C. 103(a) be withdrawn.

New claims 12-18 depend from claims 1 and 4. Thus, Applicants submit that claims 12-18 are allowable for at least the same reasons as set forth above with regard to claims 1 and 4.

For the aforementioned reasons, it is respectfully submitted that all claims pending in the present application are in condition for allowance. The Examiner is invited to contact the undersigned at (713) 934-4052 with any questions, comments or suggestions relating to the referenced patent application.

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Respectfully submitted,

  
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